MEDIUM POWER SILICON TRANSISTOR D-C TO D-C CONVERTERS

BY THOMAS B. MILLS

I. INTRODUCTION

Two small, lightweight low- and medium-power d-c to d-c converters are described along with pertinent design information. Recent advances in medium-power, high-frequency silicon transistors have made it possible to design converters with high switching frequencies which greatly reduce weight and size. The two converters described in this paper, a 50-W two-transistor circuit and a 100-W four-transistor circuit are shown in Fig. 1. The 50-W unit measures 2-1/2" x 2-3/4" x 1-1/2" and weighs 9 oz.; the 100-W unit measures 3" x 3" x 1-1/2" and weighs 12 oz. Their performance specifications are given in Table 1.

TABLE I

PERFORMANCE SPECIFICATIONS

	50-W	100-W
Input Voltage (d-c)	25V	25 V
Output Voltage (d-c)	250 V	250 V
Input Current (d-c)	2.8 A	6.0 A
Output Current (d-c)	200 mA	400 mA
Output Voltage Ripple (d-c)	$\leq$ 0.5%	$\leq$ 0.5%
Output Impedance	70 Ω	70 Ω
Operating Frequencies	50 Kc	50 Kc
Efficiency	85%	85%

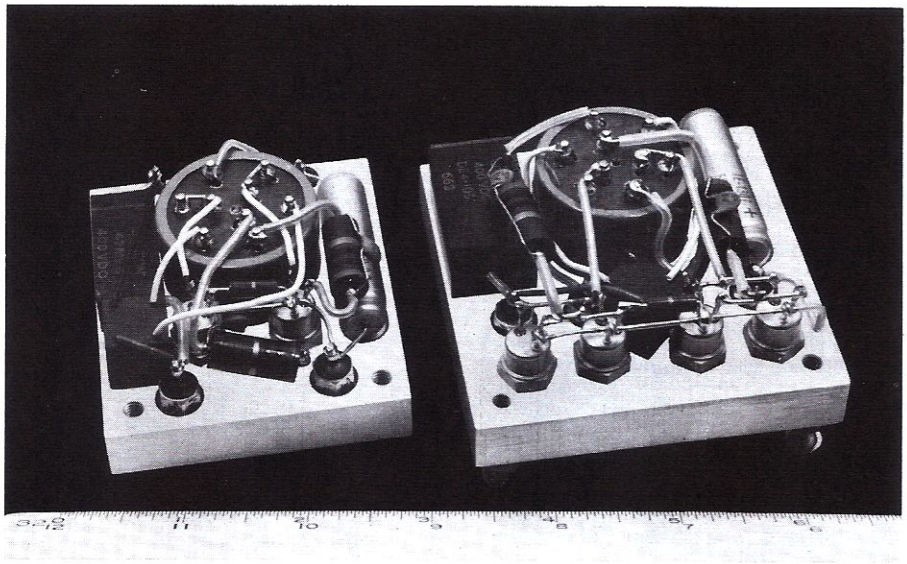

FIG. 1. A 50 W converter (left) and a 100 W converter (right).

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The devices which have made these supplies possible are the 2N2892/2N2893 30-W planar silicon transistors. They can provide higher power outputs at higher switching speeds than previously available power switches. A summary of their characteristics is given in Table II.

feedback on the base winding assures that Q_1 will remain on, while the other half of the feedback winding maintains a back bias on Q_2 keeping it turned off. Since the voltage across the core is essentially the battery voltage, a square pulse (one-half of the square-wave cycle) appears at the output.

TABLE II

Symbol	2N2893	2N2892	Units	Test Conditions
T_J	200	200	°C max	Operating
P_D	30	30	W max	Total at 25°C Case Temperature
V_{CEO}	80	80	V max	
h_{FE}	75	50	typ	I_C = 2 A, V_{CE} = 5 V
h_{fe} (20 mc)	2.5	2.3	typ	I_C = 200 mA, V_{CE} = 10 V
I_{CEX}	100	100	nA max	V_{CE} = 60 V, V_{BE} = -2 V, 25°C

Both converters use the same type of circuit and parts except for the two additional transistors in the higher-power version; therefore, all basic information applies to both units.

II. CIRCUIT DESCRIPTION

The circuits of the 50- and 100-W converters are shown in Figs. 2 and 3, which are identical except for the additional transistors and bias resistors used in the high-powered unit. Circuit operation is as follows: Assuming the condition when Q_1 turns on, the full supply voltage is applied across one-half of the transformer primary; regenerative

When the core reaches saturation, its magnetizing inductance drops rapidly, causing a rapid collector current increase in Q_1; the voltage across the primary decreases at this time causing less feedback voltage, thus less feedback current to Q_1. When an equilibrium is approached such that $I_C = h_{fe} \times I_B$, the transistor comes out of saturation. At this point, the voltage across the primary falls very rapidly and reverses polarity due to the inductive "kick" effect of the leakage inductance between the primary and feedback windings. Switching occurs at this time; Q_1 is turned off and Q_2 rapidly turns

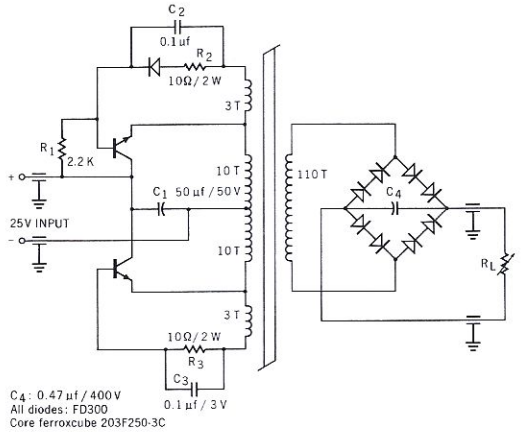

FIG. 2. Schematic diagram of the 50 W d-c to d-c converter.

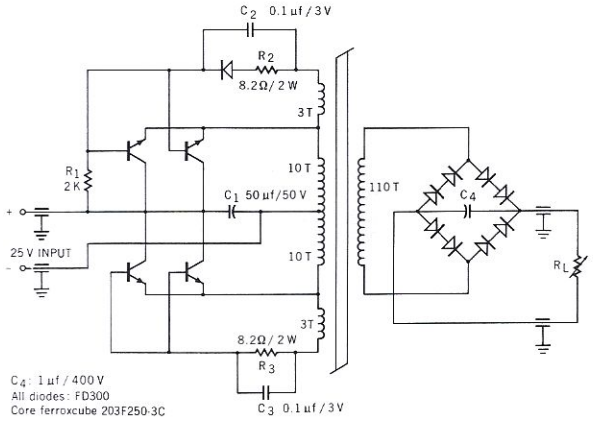

FIG. 3. Schematic diagram of the 100 W d-c to d-c converter.

on, repeating the cycle. The waveform across the output winding of the transformer is essentially a square wave which is rectified by diodes D_1 through D_8 and filtered by C_4.

III. DESIGN CONSIDERATIONS

The first step in the design of the converter is to determine the input-output requirements. In most cases, the load voltage and current have been established, giving the output power; and also the input voltage has been specified. Thus only the input current must be calculated. This can be found by assuming a value of efficiency and applying it to the output power. In the two converters described, an efficiency of 80% was assumed, which turned out to be quite close to that actually obtained. For the low-power converter

$$P_{OUT} = 50\ W,\ E_{IN} = 25\ V \qquad (1)$$

therefore,

$$I_{IN} = \frac{50\ W}{25\ V \times 0.8} = 2.5\ A \qquad (2)$$

For the medium-power unit, in which

$$P_{OUT} = 100\ W,\ E_{IN} = 25\ V$$

then

$$I_{IN} = \frac{100}{25 \times 0.8} = 5\ A \qquad (3)$$

From the 2N2891/2N2893 data sheet, it will be noted that there is a rapid decline of current gain above I_C = 3 A, and a rapid increase of base saturation voltage above I_C = 3 A; also, collector-to-emitter saturation voltage increases rapidly above this value of collector current. For these reasons, efficiency will decrease and transistor heating will increase if currents much greater than 3 A are switched by one transistor. Since primary current for the 50-W unit is only 2.5 A, only two transistors are used, while four are required for the 100-W unit.

Switching losses

Switching losses in the power transistors can be approximated by noting the collector-to-emitter current-voltage relationships and switching times involved (see Fig. 4).

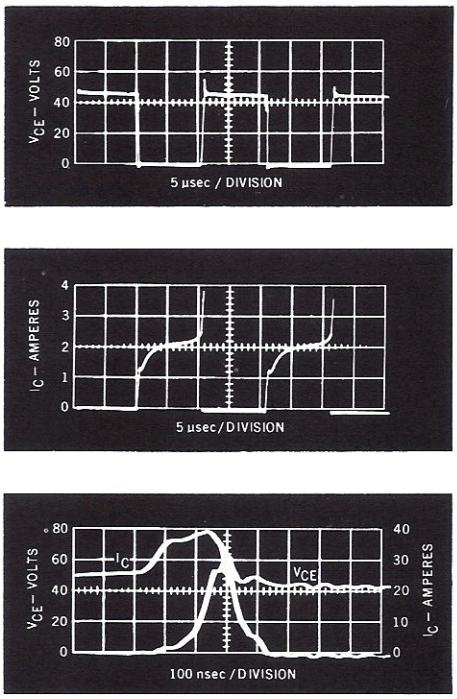

FIG. 4. Oscillogram of the voltage and current during the switching interval.

Turn-on losses appear as a very small part of total switching losses involved since the equivalent load to the transistor appears inductive. Collector current, therefore, rises relatively slowly although the collector-to-emitter voltage is quite low at this time; hence, dissipation is also low. Turn-off losses, on the other hand, are large due to the high load current plus high magnetizing current drawn by the transformer during saturation.

Immediately preceding turn-off time, the current and voltage waveforms are determined by a number of factors which include change of magnetizing inductance due to transformer saturation, leakage inductance between primary and feedback windings, load impedance, emitter-to-base transition capacitance, and the base driving network.

Several of these factors are nonlinear during the turn-off portion of the cycle, making an analysis of the transient response quite difficult. However, by observation of the collector current and voltage waveforms, we find that the collector current rises quite rapidly at core saturation to a value determined by the base current and the charge stored in the transistor base-to-emitter diffusion capacitance.

When the transformer saturates, the coefficient of coupling is decreased, causing the base current to fall; collector voltage is, therefore, beginning to rise while the collector current is still at a high value. At this time, there may typically be twice the collector current flowing than is normally drawn during the cycle, and the collector voltage will typically be more than twice the supply voltage, causing very high peak dissipation. To maintain good efficiency, the time during which the transistor is switching off must represent a very small portion of the operating cycle.

Transformer losses

Transformer losses also increase with operating frequency. Two types of transformer losses must be considered: core and copper (wire) loss. Core loss can be divided into hysteresis loss and eddy-current loss. Hysteresis loss increases linearly with frequency since it represents the energy per cycle required to traverse the hysteresis loop (magnetize and demagnetize) the core material. Eddy-current loss per cycle is a function of the operating frequency and, hence, goes up proportionally to an exponential of 2 with increasing frequency.

Mathematically, these losses can be summed on a per-cycle basis

$$P_c/f = K_1 + K_2 f$$

where

P_c = total core loss
K_1 = a constant equal to hysteresis loss
K_2 = a constant equal to one-cycle eddy-current loss
f = frequency

Depending upon which of these terms predominates around the frequency range of interest, core loss will increase linearly or exponentially with frequency.

Hysteresis loss is a function of the area of the hysteresis loop of the core material, while eddy-current losses are a function of the resistivity of the core material and lamination thickness and insulation between laminations in tape or stacked cores.

Losses in thin-tape wound cores of permalloy type material are predominately due to eddy currents above a few hundred cycles per second while losses in ferrite materials are largely hysteresis losses below a few hundred kilocycles per second.

In the frequency range of the converter described, the theoretical losses for good quality ferrite and 1-mil permalloy tape cores are essentially the same for a given core volume, being approximately 2 to 4 W per cm^3 at the chosen 50 Kc.

Another factor to be considered is the behavior of the core during saturation, and how this affects the switching time of the transistors. Experimental observations of transformers operating in the 50-Kc region show that ferrite materials provide faster switching, due to lower core losses at high frequencies associated with switching. In a typical converter, a good quality permalloy tape core showed a turn-off time of 300 nsec, while a ferrite core showed approximately 100 nsec.

Copper losses do not increase appreciably in the frequency range of interest, but experience has shown that it is advisable to use as few turns of wire as possible to reduce winding capacitance, which will cause high charging currents in the transformer and hinder proper switching of the transistors.

Operating frequency

An optimum frequency of operation can be determined from an analysis of overall converter loss with consideration of component weight and size. As the operating frequency is increased, size and weight of the power transformer and filter components will decrease, but circuit loss will increase. So it becomes a trade of size and weight vs. efficiency. In the design considered here, 50 Kc was considered an optimum frequency due to excessive core heating and switching loss above this frequency. Operation at a lower frequency would mean larger components and only a small gain in efficiency.

Circuit design

The converter design can be started after an operating frequency has been chosen, and the input-output voltage and currents are known.

The first step is to determine the type and size of the core. Only toroidal cores were considered for the described converters because of the lack of an air gap in this configuration. The use of an air-gapped structure would result in a reduction of squareness ratio and, hence, an increase in magnetizing current.

The fundamental equation in transformer design, derived in Appendix A, relates the voltage on a core winding to the flux in the core

$$E = -4fNB_{max}A \times 10^{-8} \qquad (5)$$

where

- E = core voltage in volts
- f = operating frequency in cps
- N = number of turns on winding
- B_{max} = saturation flux density in gauss
- A = core area in cm^2

At first glance, there appears to be an extremely wide range of values of flux density, core area, and number or turns that will satisfy this equation for a given supply voltage and frequency. Certain narrowing limits will soon become apparent in the design of the high-frequency transformer. Regrouping the terms of Eq. (5) assists in the evaluation

$$E/N = 4 B_{max} Af \times 10^{-8} \qquad (6)$$

To reduce winding capacitance, the number of turns on the core should be as small as possible; however, there must be sufficient turns to insure good coupling to the core, i.e., too small a number of turns would not cover enough volume of the toroid to produce a defined amount of flux change. A value of approximately 2.5 V per turn for E/N gives satisfactory results at these frequencies.

After selecting the core material, frequency of operation, supply voltage, and number of turns, the core area can then be selected. Choosing Ferroxcube 3 C material for the core,

$$B_{max} \simeq 3.4\,K \text{ gauss} \qquad (7)$$

$$2.5 \text{ V/turn} = 4 \times 3.4 \times 10^3 \text{ gauss} \times A \times 50 \times 10^3 \text{ cps} \times 10^{-8}$$

$$A = \frac{2.5}{4 \times 3.4 \times 50} \times 10^{-2} = 0.37\,cm^2 \qquad (8)$$

The nearest size available is $0.404\,cm^2$; therefore, using this area, and 10 turns,

$$f = \frac{25 \text{ V} \times 10^8}{4 \times 3.4 \times 10^3 \times 0.404 \times 10} = 45.5 \text{ Kc} \qquad (9)$$

Since each transistor switches the supply voltage alternately across each half of the primary, the 10 turns are needed on each side of the primary center tap.

It was found on several experimental transformers that high-frequency oscillation (in the 10-Mc range) occurred in the off transistor when the feedback winding was placed close to or on top of the emitter winding. The most satisfactory placement of wire on the core is shown in Fig. 5.

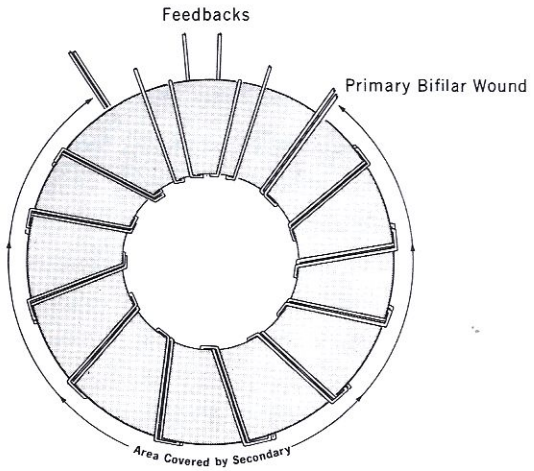

FIG. 5. Recommended winding configuration of the power transformer.

In this configuration, the feedback windings are some distance from the main winding which alleviates the problem of oscillation due to excess phase shift in the off transistor in the 10-Mc region.

The feedback winding, N_2, can be found from the turns ratio

$$E_{fb} = E_{supply}\, N_2/N_1 \qquad (10)$$

It is desirable to establish a base current rather than a voltage, so E_2 should be chosen large enough to provide sufficient drop across a resistor to establish this current, but smaller than the reverse V_{be} breakdown of the transistor. The amount of base current necessary is that needed to establish saturation of the transistor at whatever supply current is being drawn. This amounts to 2.5 A per transistor for either converter. Assuming a minimum $h_{fe}(sat)$ of 6 at I_C = 2.5 A, $I_b \simeq 415$ mA, choosing N_2 = 2 turns, then E_{fb}, the voltage fed back on winding N_2

$$E_{fb} \simeq E_{supply}\, N_2/N_1 = \frac{25 \times 2}{10} = 5\,V \qquad (11)$$

$$R_{2,3} = \frac{E_{fb} - V_{be}}{I_b} = \frac{5\,V - 1\,V}{415\ mA} \simeq 10\,\Omega \qquad (12)$$

For the 100-W converter, two transistors are used in parallel, and, hence, the current fed back from the transformer will be twice that in the 50-W converter. To maintain a fairly large value of R_1, another turn is used on the feedback winding, so

$$E_{fb} = 25\,V \times 3/10 = 7.5\,V \qquad (13)$$

$$R_1 = \frac{7.5\,V - 1\,V}{830\ mA} = 7.9\,\Omega \qquad (14)$$

In practice, the values shown in Figs. 2 and 3 were chosen.

Capacitors C_2 and C_3 are used to speed up the turn-on and turn-off times of the transistor. The value of these capacitors depends upon the value of R_1, the base-to-emitter diffusion capacitance, various stray capacitances in the transformer, and leakage inductances in the transformer. Since some of these factors are nonlinear during switching, the value of these capacitors is best determined by experiment. The values shown proved satisfactory, and contribute approximately 10% greater efficiency over the case where no capacitor is used.

The output winding of the transformer can be found from

$$E_o = E_{IN} \times N_3/N_1 \qquad (15)$$

where E_{IN} is the voltage applied to the winding. This will be lower than the 25-V supply due to transistor saturation losses and I^2R losses in the winding.

C_1 is connected across the battery input terminals to provide a low impedance source to drive the power transformer. This capacitor also reduces feedback ripple to the power supply. The

value of this capacitor is dependent upon the battery source impedance at the operating frequency, but it is not critical in value as long as it is large enough to provide a stiff voltage source.

Diode considerations and calculations

Fairchild FD300 diodes were chosen for the power rectifiers because of their high-speed and current handling capabilities. The output current required from the medium-power converter is 400 mA. The average forward current rating of the FD300 diode is 300 mA; and since any particular diode is required to carry 400 mA for one-half the time, the average current through each unit is only 200 mA, or two-thirds that of rated value.

Since there are four diodes in series in each forward direction of the bridge, the power loss in the diodes may be calculated

$$P_{loss} = \frac{(8 \times 0.4\,A \times 1.1\,V)}{2} = 1.75\,W \qquad (16)$$

The power loss in each diode is then one-eighth of this value, since there are eight diodes

$$P_{per\ diode} = 1/8 \times 1.75\,W = 0.219\,W \qquad (17)$$

The inverse voltage across each diode can be found by remembering in the reverse bridge direction: there are four diodes in series, and twice the d-c output voltage is impressed across the diodes; therefore,

$$E_{inverse/diode} = \frac{2 \times 250}{4} = 125\,V \qquad (18)$$

Since the working inverse voltage of the FD300 is 125 V, it was decided to select diodes with breakdowns greater than 175 V to allow a margin of safety. The eight diodes required were packaged in a molded block which is designated the FA364 diode bridge.

Filter design

The filter circuit, consists of C_4, the source resistance composed of diode resistance, transformer secondary resistance, reflected primary resistance, and the load resistance R_L.

From available data,[1] the percentage of ripple can be determined in terms of the above parameters and the operating frequency. Since this data is given for sinusoidal waveforms, the results obtained will be pessimistic when used for a square-wave case; however, they do provide a first order approximation that is helpful.

For 0.5% ripple, with $R_{source}/R_{load} = 0.1\%$, an ωCR_L product of 160 is obtained.

Since $R_L = \frac{(250\,V)^2}{100\,W}$ for the medium power unit, and

$$\omega = 2\pi \times 50\,Kc = 314 \times 10^3\,rad/sec$$

$$C = \frac{160}{314 \times 10^3 \times 625} = 0.8\,\mu f \qquad (19)$$

The ripple referred to above is predominantly due to fundamental components, and some trouble may be experienced with high-frequency ringing associated with switching. This may be quite high in frequency in the 5 to 10 Mc region, and r-f filtering techniques may have to be used to reduce it.

Thermal considerations

The problem of heat dissipation in the design of the two converters is very important due to the small component and chassis size. The 50-W unit generates approximately 10 W of heat, while the 100-W unit generates approximately 18 W of heat.

The dissipation in each power transistor can be divided into saturation losses and switching losses. Saturation losses can be found from

$$P_{SAT} = 1/2\ V_{CE}(sat)\, I_C \qquad (20)$$

for the 50-W converter

$$= 1/2\ (0.5\,V)\ 2.5\,A$$

$$\simeq 0.6\,W/\text{transistor}$$

A factor of 1/2 is used since each transistor is on for one-half of one full cycle. Switching losses are only important during turn off, and can be determined from Fig. 4, which shows the current voltage relations during this time; and finding the average power during the switching interval T_s, from the formula derived in Appendix B,

$$P_{T_s}(\text{avg}) = 1/2\, V_{CE}(\text{peak})\, I_C(\text{peak})$$

$$= 1/2\ \ 50 \times 3.8\,A$$

$$= 95\,W \qquad (21)$$

This is dissipation during the switching interval of 220 nsec, since a full cycle is 20 μsec,

$$P\,(\text{avg}) = 95\,W \times \frac{0.22}{20} \simeq 1.0\,W \qquad (22)$$

This is the average power per transistor due to switching.

An additional source of heating in the base-emitter junction, since

$$V_{BE}(\text{sat}) \simeq 1.0\,V \text{ at } I_b = 400\,mA,\ P_{BE} = 0.4\,W$$

Summing all losses in the transistor

$$P_{\text{Total}} = 0.6 + 1 + 0.4 = 2.0\,W$$

For both transistors, this becomes 4 watts

The power loss in the transformer is essentially in the core and is estimated at 3 W from manufacturers' data at 50 Kc. Due to this relatively large amount of heat in toroid, it is mounted in a metal can and the can is filled with high-heat conductance epoxy. Mounting studs bolt from the can to the main heat sink. Miscellaneous losses in diodes, feedback resistors, etc., amount to approximately 2 W, giving a total overall converter loss of 9 W.

A similar analysis of the 100-W converter will show transistor losses are approximately doubled; while resistive losses are quadrupled, transformer losses probably remain the same.

CONCLUSION

It is feasible to design high frequency dc-dc or dc-ac converters at high switching frequencies using the 2N2891/2N2893 high-speed, silicon power transistors. A slight sacrifice in efficiency is encountered over lower frequency converters, but substantial savings in power and weight are realized.

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ACKNOWLEDGEMENT

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APPENDIX A

Derivation of Transformer Equation

The relationship between core flux and impressed voltage can be found from

$$e = -N \frac{d\phi}{dt}$$

where

e = instantaneous voltage
ϕ = instantaneous flux in the core
N = number of turns on the core

rearranging terms

$$edt = -Nd\phi \qquad (1\text{-}A)$$

Remembering that we are impressing the entire supply voltage (minus wire and transistor saturation losses) across N turns of the primary, the total flux change can be found by integrating (1-A)

$$e \int_0^{T/2} dt = -N \int_{-\phi_{max}}^{+\phi_{max}} d\phi$$

The limits are chosen such that $T = 1/f$ or $1/2$ cycle time $= T/2$, and the total flux switched is $2\phi_{max}$, since we are starting the cycle at $-\phi_{max}$ and going to $+\phi_{max}$

$$E\left[T/2 - 0\right] = -N\left[\phi_{max} + \phi_{max}\right]$$

or

$$ET = -4N\phi_{max}$$

letting $f = 1/T$

$$E = -4f\ N\phi_{max}$$

since $\phi = BA$, and adding a factor of 10^{-8} to make the various terms compatible in the cgs system of units

$$E = -4f\ NB_{max}A \times 10^{-8} \qquad (2\text{-}A)$$

where

E = core voltage in volts
f = operating frequency in cps
N = number of turns on primary
B_{max} = saturation flux density in gauss
A = core area in cm^2.

APPENDIX B

Determination of turn-off losses:

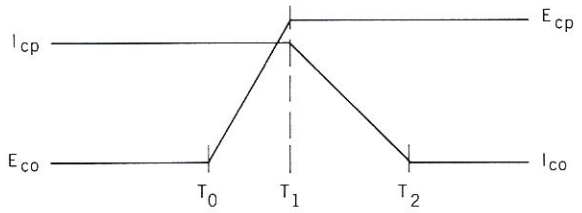

FIG. B1. Idealized current-voltage waveform.

Assuming an idealized current voltage waveform shown in Fig. B1, where I_C remains constant and V_{CE} rises linearly to some peak value, at which time V_{CE} remains constant and I_C falls linearly to zero, the average power during switching is

$$P(avg)\,T_s = \frac{1}{T_s}\left[\int_{T_o}^{T_1} I_{cp}E_{cp}\,\frac{t}{T_1 - T_o}\,dt + \int_{T_1}^{T_2} E_{cp}I_{cp}\left(1 - \frac{t}{T_2 - T_1}\right)dt\right]$$

$$= \frac{E_{cp}I_{cp}}{T_s}\left\{\left[\frac{1}{2}\,\frac{t^2}{T_1 - T_o} + \right]_{T_o}^{T_1} \left[t - \frac{1}{2}\,\frac{t^2}{T_2 - T_1}\right]_{T_1}^{T_2}\right\}$$

$$= \frac{E_{cp}I_{cp}}{T_s}\left[\frac{1}{2}\left(T_1 - T_o\right) + \left(T_2 - T_1\right) - \frac{1}{2}\left(T_2 - T_1\right)\right]$$

$$= \frac{E_{cp}I_{cp}}{T_s} \times \frac{1}{2}\left(T_2 - T_o\right)$$

since $T_s = T_2 - T_o$

$$P(avg)\,T_s = 1/2\,E_{cp}I_{cp}$$